IN THE CLAIMS

1.(Currently Amended) A semiconductor die comprising:

means ~~a conductive test signal bump~~ for transmitting test signals off of said semiconductor die;

means ~~a test signal redistribution layer trace~~ for communicating said test signals to said means for transmitting test signals off of said semiconductor die ~~conductive test signal bump~~, wherein said means for communicating said test signals to said means for transmitting test signals off of said semiconductor die ~~test signal redistribution layer trace~~ is routed in a spiral pattern included in a redistribution layer and said means for communicating said test signals to said means for transmitting test signals off of said semiconductor die ~~test signal redistribution layer trace~~ is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said means for communicating said test signals to said means for transmitting test signals off of said semiconductor die, said test signal redistribution layer trace communicatively coupled to said conductive test signal bump; and

means ~~a test probe point~~ for accessing said test signals in said semiconductor die and for electrical coupling a conductor to said redistribution layer.

2.(Original) The semiconductor die of Claim 1 wherein said semiconductor die is a flip chip die configured for connection to a package substrate such that said conductive test signal bump is electrically coupled to an external access point of said package substrate.

3.(Original) The semiconductor die of Claim 1 wherein said test probe point is accessible by drilling from a first surface of said semiconductor die.

4.(Previously Presented) The semiconductor die of Claim 1 wherein said test probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill, wherein said FIB pad is communicatively coupled to said test signal redistribution layer trace by said conductive material backfill.

5.(Previously Presented) The semiconductor die of Claim 1 wherein said test signal redistribution layer trace is dedicated for test signals.

6. (Cancelled)

7.(Previously Presented) The semiconductor die of Claim 1 wherein said test

signal redistribution layer trace is routed in said spiral pattern with conductive fingers located in positions such that drilling and conductive material backfill provides access to internal signals for testing at various electronic component configuration granularity.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Previously Presented) A semiconductor device comprising:

means ~~a package substrate~~ for communicating test signals on an external access point, wherein said means for communicating test signals on an external access point is a package substrate ~~package substrate includes a conductive trace disposed such that multiple test signals are accessible at varying degrees of~~

~~electronic component granularity within said package substrate and along said conductive trace~~; and

a semiconductor die having test probe points accessible by said external access point, wherein said semiconductor die is electrically coupled to said package substrate, wherein said semiconductor die comprises:

~~a conductive test signal bump~~ means for transmitting internal test signals off of said semiconductor die to said package substrate, means for transmitting internal test signals off of said semiconductor die to said package substrate is a conductive test signal bump, said conductive test signal bump is located on a first surface of said semiconductor die and electrically coupled to ~~said~~ a signal redistribution layer;

means ~~a redistribution layer including a test signal redistribution layer trace~~ for communicating internal signals to said conductive test signal bump, wherein said means for communicating internal signals to said conductive test signal bump is a redistribution layer including a test signal redistribution layer trace, wherein said test signal redistribution layer trace is routed in a spiral pattern included in a redistribution layer and said test signal redistribution layer trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said test signal

redistribution layer trace, said trace signal redistribution layer communicatively coupled said conductive test signal bump;

means ~~a test probe point~~ for accessing test signals in said semiconductor die and for electrical coupling to said signal redistribution layer, wherein said means for accessing test signals in said semiconductor die and for electrical coupling to said signal redistribution layer is a test probe point; and

means ~~a test access via~~ for electrically coupling said test probe point to said signal redistribution layer, wherein said means for electrically coupling said test probe point to said signal redistribution layer is a test access via.

14.(Currently Amended) The semiconductor device of Claim 13 wherein said package substrate comprises:

a first surface with ball grid array;

a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die, including a conductive contact for electrically coupling with a conductive test signal bump; and

a means ~~trace~~ for electrically coupling one of said conductive contacts to said external access point, wherein said means is a trace.

15. (Cancelled)

16.(Previously Presented) The semiconductor device of Claim 13 wherein said test probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill.

17.(Previously Presented) The semiconductor device of Claim 13 wherein said test signal redistribution layer trace is routed in patterns in which trace widths and spacing between redistribution layer traces are minimized without causing signal interference.

18.(Original) The semiconductor device of Claim 14 wherein said external access point is accessible by automatic test equipment.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled) A semiconductor device comprising:

a package substrate for communicating test signals on an external access point; and

a semiconductor die having test probe points accessible by said external access point, wherein said semiconductor die is electrically coupled to said package substrate, wherein said semiconductor die comprises:

a conductive test signal bump for transmitting internal test signals off of said semiconductor die to said package substrate, said conductive test signal bump located on a first surface of said semiconductor die and electrically coupled to ~~said~~ a signal redistribution layer;

a redistribution layer including a test signal redistribution layer

trace for communicating internal signals to said conductive test signal bump, wherein said test signal redistribution layer trace is routed in a spiral pattern and said test signal redistribution layer trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said test signal redistribution layer trace, said test signal redistribution layer trace communicatively coupled to said conductive test signal bump;

said signal redistribution layer communicatively coupled said conductive test signal bump;

a test probe point for accessing test signals in said semiconductor die and for electrical coupling to said signal redistribution layer; and

a test access via for electrically coupling said test probe point to said signal redistribution layer.

37.(Previously Presented) The semiconductor device of Claim 36 wherein said test signal redistribution layer trace is routed in said spiral pattern with conductive fingers located in positions such that drilling and conductive material backfill provides access to internal signals for testing at various electronic component configuration granularity.

38. (Currently Amended) The semiconductor device of Claim 36 wherein said semiconductor die ~~package substrate~~ comprises a conductive trace disposed such that said test signals are accessible at varying degrees of electronic component granularity.

39. (Previously Presented) The semiconductor device of Claim 36 wherein said package substrate comprises:

a first surface with ball grid array;

a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die, including a conductive contact for electrically coupling with a conductive test signal bump; and

a means ~~trace~~ for electrically coupling one of said conductive contacts to said external access point.

40. (Previously Presented) The semiconductor device of claim 36 wherein said test signal is a semiconductor die signal while said semiconductor die is operating.